IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method of processing data in a programmable processor, the method comprising:

decoding a single instruction for selectively arranging data, specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

2. (currently amended) The method of claim 1 wherein each field of the data selection operand provides a sufficient number of bits to specify ~~anyone~~ any one of the plurality of data elements.

3. (original) The method of claim 2 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements.

4. (original) The method of claim 1 wherein the data selection operand is provided by a register specified by the single instruction.

5. (original) The method of claim 4 wherein the data selection operand has a width equal to the specified register width.

6. (original) The method of claim 1 wherein the catenated result is provided to a register.

7. (original) The method of claim 1 wherein the plurality of data elements has a combined width equal to the width of the first register plus the width of the second register.

8. (original) The method of claim 1 wherein the instruction further specifies a data element width of the plurality of data elements.

9. (original) The method of claim 1 wherein each data element has a width of 8 bits.

10. (original) The method of claim 1 wherein the catenated result has a width of 128 bits.

11. (original) The method of claim 1 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

12. (currently amended) The method of claim 1 further comprising:

decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or of products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

13. (original) A method for selectively arranging data in a programmable processor, the method comprising:

decoding a single instruction specifying a data selection operand and a first register having a register width, the first register providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

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for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

14. (original) A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

15. (currently amended) The computer-readable medium of claim 14 wherein each field of the data selection operand provides a sufficient number of bits to specify ~~anyone~~ any one of the plurality of data elements.

16. (original) The computer-readable medium of claim 15 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements.

17. (original) The computer-readable medium of claim 14 wherein the data selection operand is provided by a register specified by the single instruction.

18. (original) The computer-readable medium of claim 17 wherein the data selection operand has a width equal to the specified register width.

19. (original) The computer-readable medium of claim 14 wherein the catenated result is provided to a register.

20. (original) The computer-readable medium of claim 14 wherein the plurality of data elements has a combined width equal to the width of the first register plus the width of the second register.

21. (original) The computer-readable medium of claim 14 wherein the instruction further specifies a data element width of the plurality of data elements.

22. (original) The computer-readable medium of claim 14 wherein each data element has a width of 8 bits.

23. (original) The computer-readable medium of claim 14 wherein the catenated result has a width of 128 bits.

24. (original) The computer-readable medium of claim 14 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

25. (currently amended) The computer-readable medium of claim 14 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

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multiplying the plurality of floating point operands in the third register by the plurality of

operands in the fourth register to produce a plurality ~~or~~ <u>of</u> products; and

providing the plurality of products to partitioned fields of a result register as a catenated

result.

26. (original) A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for

selectively arranging data in a programmable processor, the group element selection instruction

capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection

operand and a first register having a register width, the first register providing a plurality of data

elements each having an elemental width smaller than the register width, the data selection

operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by

the field to a predetermined position in a catenated result.

Claims 27-39. (cancelled)

40.   (New) A method of processing data in a programmable processor, the method

comprising:

decoding a single instruction specifying a plurality of registers storing a plurality of 8-bit

data elements, an index register storing an index vector comprising a plurality of equal-sized

selectors stored in partitioned fields of the index register and a destination register; and

for each selector in the index vector, providing a data element selected by the selector to

a predetermined position in the destination register.

41.   (New) The method set forth in claim 40 wherein the plurality of registers comprises two registers.

42.   (New) The method set forth in claim 40 wherein the plurality of registers comprises two 64-bit registers storing a combined total of sixteen 8-bit data elements.

43.   (New) The method set forth in claim 40 wherein the number of selectors stored in the index register is equal to the number of predetermined positions in the destination register.

44.   (New) The method set forth in claim 40 wherein the index register is a 64-bit register.

45.   (New) The method set forth in claim 40 wherein the index vector comprises n equal-sized selectors and the destination register comprises n equal-sized predetermined positions.

46.   (New) The method set forth in claim 45 wherein the selector stored in a lowest order set of bits of the index register provides a data element to a lowest order set of bits of the destination register, the selector in a second lowest order set of bits of the index register provide a data element to a second lowest order set of bits of the destination register and the selector stored in a highest order set of bits of the index register provides a data element to a highest order set of bits of the destination register.

47.   (New) The method set forth in claim 40 wherein the destination register is a 128-bit register.

48.   (New) The method set forth in claim 40 wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector.

49.   (New) The method set forth in claim 40 wherein the index register stores sixteen 4-bit selectors.

50.   (New) A method of processing data in a programmable processor, the method comprising:

decoding a single instruction specifying a first register storing a first plurality of 8-bit data elements, a second register storing a second plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register;

for each selector in the index vector, providing a data element from one of the first or second plurality of 8-bit data elements selected by the selector to a predetermined 8-bit position in the destination register, wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register.

51.   (New) The method set forth in claim 50 wherein the first and second registers are 64-bit registers, the index register is a 64-bit register and each selector stored in the index register has a sufficient number of bits to select any one of the 8-bit data elements in the first or second pluralities of 8-bit data elements.

52.   (New) The method set forth in claim 50 wherein the destination register is a 128-bit register.

53.   (New) The method set forth in claim 50 wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector.

54.   (New) A computer-readable medium having stored therein a plurality of instructions that cause a computer processor having registers to perform operations on data elements stored in registers within the processor, the plurality of instructions comprising:

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an instruction specifying a plurality of registers storing a plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register; and

wherein for each selector in the index vector, the instruction causes the computer processor to provide a data element selected by the selector to a predetermined position in the destination register.

55.   (New) The computer-readable medium set forth in claim 54 wherein the plurality of registers comprises two registers.

56.   (New) The computer-readable medium set forth in claim 54 wherein the plurality of registers comprises two 64-bit registers storing a combined total of sixteen 8-bit data elements.

57.   (New) The computer-readable medium set forth in claim 54 wherein the number of selectors stored in the index register is equal to the number of predetermined positions in the destination register.

58.   (New) The computer-readable medium set forth in claim 54 wherein the index register is a 64-bit register.

59.   (New) The computer-readable medium set forth in claim 54 wherein the index vector comprises n equal-sized selectors and the destination register comprises n equal-sized predetermined positions.

60.   (New) The computer-readable medium set forth in claim 59 wherein the selector stored in a lowest order set of bits of the index register provides a data element to a lowest order set of bits of the destination register, the selector in a second lowest order set of bits of the index register provide a data element to a second lowest order set of bits of the destination register and

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the selector stored in a highest order set of bits of the index register provides a data element to a highest order set of bits of the destination register.

61. (New) The computer-readable medium set forth in claim 54 wherein the destination register is a 128-bit register.

62. (New) The computer-readable medium set forth in claim 54 wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector.

63. (New) The computer-readable medium set forth in claim 54 wherein the index register stores sixteen 4-bit selectors.

64. (New) A computer-readable medium having stored therein a plurality of instructions that cause a computer processor having registers to perform operations on data elements stored in registers within the processor, the plurality of instructions comprising:

an instruction specifying a first register storing a first plurality of 8-bit data elements, a second register storing a second plurality of 8-bit data elements, an index register storing an index vector comprising a plurality of equal-sized selectors stored in partitioned fields of the index register and a destination register; and

wherein for each selector in the index vector, the instruction causes the computer processor to provide a data element from one of the first or second plurality of 8-bit data elements selected by the selector to a predetermined 8-bit position in the destination register, wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register.

65. (New) The computer-readable medium set forth in claim 64 wherein the first and second registers are 64-bit registers, the index register is a 64-bit register and each selector stored

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in the index register has a sufficient number of bits to select any one of the 8-bit data elements in the first or second pluralities of 8-bit data elements.

66.   (New) The computer-readable medium set forth in claim 64 wherein the destination register is a 128-bit register.

67.   (New) The computer-readable medium set forth in claim 64 wherein each of the equal-sized selectors stored in partitioned fields of the index register is a 4-bit selector.